App. No. 09/894,205
Office Action Dated May 13, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Claims 25, 27, and 42 are amended.

Listing of Claims:

1-24. (Canceled)

25. (Currently Amended) A data processing device programmed for reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion ~~programmed~~ for reading in a computational instruction;

a decoding portion ~~programmed~~ for decoding the computational instruction that has been read in;

an execution portion ~~programmed~~ for executing the computational instruction in accordance with a decoding of the computational instruction;

a sequencer ~~programmed~~ for updating an output to one of at least three different states as a conditional execution status in response to [[an]] each instruction decoding operation among the computational instruction and subsequent instructions including a plurality of instructions that are sequentially arranged as an instruction sequence after the computational instruction; and

an instruction overriding control circuit ~~programmed~~ for controlling an overriding of any instruction of the subsequent instructions in response to the conditional execution status updated by the sequencer.

26. (Previously Presented) The data processing device according to claim 25, wherein the instruction overriding control circuit overrides none of the subsequent instructions in response to a value of a status flag determined by execution of the computational instruction regardless of the conditional execution status updated by the sequencer.

27. (Currently Amended) A data processing device programmed for reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion ~~programmed~~ for reading in a computational instruction;

a decoding portion ~~programmed~~ for decoding the computational instruction that has been read in;

an execution portion ~~programmed~~ for executing the computational instruction in accordance with a decoding of the computational instruction;

a sequencer ~~programmed~~ for updating an output to one of at least three different states as a conditional execution status in response to [[an]] each instruction decoding operation among the computational instruction and subsequent instructions including a plurality of instructions that are sequentially arranged as an instruction sequence after the computational instruction; and

an instruction overriding control circuit ~~programmed~~ for overriding at least one instruction of the subsequent instructions, the at least one instruction designated in response to a value of a status flag determined by execution of the computational instruction and the conditional execution status updated by a the sequencer.

28. (Previously Presented) The data processing device according to claim 27, wherein the instruction overriding control circuit overrides the at least one instruction by overriding an execution of the at least one instruction in the execution portion.

29. (Canceled)

30. (Previously Presented) The data processing device according to claim 27, wherein the subsequent instructions include a first instruction and a second instruction, and the computational instruction, the first instruction, and the second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides one of the first instruction and the second instruction when the status flag takes a given value.

31. (Previously Presented) The data processing device according to claim 30, wherein the instruction overriding control circuit overrides another one of the first instruction and the second instruction when the status flag takes a different value from the given value.

32. (Previously Presented) The data processing device according to claim 30, wherein each of the first instruction ~~nor~~ and the second instruction does not have any condition for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

33. (Previously Presented) The data processing device according to claim 27, wherein the subsequent instructions include a first instruction group including a plurality of instructions and a second instruction group including a plurality of instructions, and the computational instruction, the first instruction group, and the second instructional group are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides one of the first instruction group and the second instruction group when the status flag takes a given value.

34. (Previously Presented) The data processing device according to claim 33, wherein the instruction overriding control circuit overrides another one of the first instruction group and the second instruction group when the status flag takes a different value from the given value.

35. (Previously Presented) The data processing device according to claim 33, wherein any instruction included in both the first instruction group and the second instruction group does not have any condition for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

36. (Previously Presented) The data processing device according to claim 27, wherein the subsequent instructions include a first instruction and a second instruction, and the computational instruction, the first instruction, and the second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides only the first instruction only when the status flag takes a given value.

37. (Canceled)

38. (Previously Presented) The data processing device according to claim 36, wherein the first instruction does not have any condition for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

39. (Previously Presented) The data processing device according to claim 27, wherein the subsequent instructions include a first instruction group including a plurality of instructions and a second instruction group including a plurality of instructions, and the computational instruction, the first instruction group, and the second instruction group are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides only the first instruction group only when the status flag takes a given value.

40. (Canceled)

41. (Previously Presented) The data processing device according to claim 39, wherein any instruction in the first instruction group does not have any condition for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

42. (Currently Amended) A data processing device programmed for reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion ~~programmed~~ for reading in a computational instruction;

a decoding portion ~~programmed~~ for decoding the computational instruction that has been read in;

an execution portion ~~programmed~~ for executing the computational instruction in accordance with a decoding of the computational instruction;

a sequencer ~~programmed~~ for updating an output to one of at least three different states as a conditional execution status in response to [[an]] each instruction decoding operation among the computational instruction and subsequent instructions including a plurality of instructions that are sequentially arranged as an instruction sequence after the computational instruction; and

an instruction overriding control circuit ~~programmed~~ for overriding at least one instruction of the subsequent instructions, the at least one instruction designated in response to a value of a status flag determined by execution of the computational instruction and the conditional execution status updated by a the sequencer by allowing the fetch portion to skip reading in the at least one instruction.

43. (Previously Presented) The data processing device according to claim 42, wherein the fetch portion includes a plurality of buffers to override the at least one instruction.

44. (Previously Presented) The data processing device according to claim 42, wherein the subsequent instructions include a first instruction and a second instruction, and the computational instruction, the first instruction, and the second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides one of the first instruction and the second instruction by allowing the fetch portion to skip reading in the one of the first instruction and the second instruction when the status flag takes a given value.

45. (Previously Presented) The data processing device according to claim 44, wherein the instruction overriding control circuit overrides another one of the first instruction and the second instruction by overriding an execution of the another one of the first instruction and the second instruction in the execution portion when the status flag takes a different value from the given value.